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Review on Network on Chip Router Design

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Abstract— **With advancement in the technology in the on chip communication, requirement of faster interaction between devices is becoming vital. Network on Chip (NoC) can be one of the solutions for faster on chip communication. For efficient communication between devices of NoC, routers are needed. This paper reviews implementation of five port router. The use of router facilitated higher throughput as required for dealing with complexity of modern systems. It is mainly focused on the router design parameters on both system level including traffic pattern, network topology and routing algorithm, and architecture level including arbitration algorithm and buffer mechanism.**

Keywords- **Arbiter, Network on Chip, XY routing algorithm.**

I. INTRODUCTION

Recently Networks on Chip (NoC) is playing vital role in development in VLSI. Increasing levels of integration resulted in systems with different types of applications, each having its own I/O traffic characteristics. Since the early days of VLSI, communication within the chip dominated the die area and dictated clock speed and power consumption. Using buses is becoming less desirable, especially with the ever growing complexity of single-die multiprocessor systems. As a consequence, the main feature of NoC is the use of networking technology to establish data exchange within the chip. All links in NoC can be simultaneously used for data transmission, which provides a high level of parallelism and makes it attractive to replace the typical communication architectures like shared buses or point-to-point dedicated wires [1]. Apart from throughput, NoC platform is scalable and has the potential to keep up with the pace of technology advances.

NoC network can be modelled as a graph where in nodes, processing elements and edges are the connective links of the processing elements. Figure 1 shows the basic NoC architecture, it basically includes processing element (PE), router. Each PE is attached to NI which connects the PE to a local router. When a packet was sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via the decision made by each router.

Like in any other network, router is the most important component for the design of communication back bone of a NoC system. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. It is very important that design of a NoC router should be as simple as possible because implementation cost increases with an increase in the design complexity of a router [2].

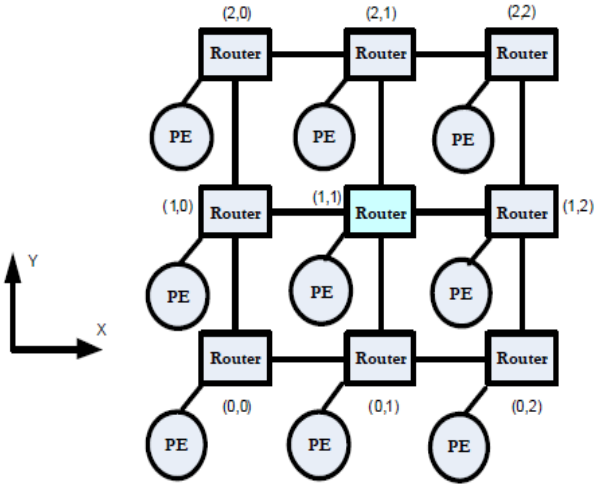

Fig.1 Basic NoC architecture with mesh topology

II. LITERTATURE SURVEY

The author illustrated the impact of repeater insertion on inter-router links with adaptive control and eliminating some of the buffers in the router. The approach saved appreciable amount of power and area without significant degradation in the throughput and latency, though there is still some scope to increase the buffer utilization inside the router [3]. Reference [4] shows work on router for NoC to increase throughput of the network and they introduced the architecture which shows a significant improvement in throughput at the expense of area and power due to extra crossbar and complex arbitration scheme. The throughput increased up to 94% but power consumption is increased by the factor of 1.28 [4].

By utilizing the buffer with bidirectional channels indicated significant improvement in system performance, though in this case, each channel controller will have two additional tasks: dynamically configuring the channel direction and to allocate the channel to one of the routers, sharing the channel. Also, there is a 40% area overhead over the typical NoC router architecture due to double crossbar design and control logic [5]. The author developed an algorithm to optimize size of decoupling buffers in network interfaces. The buffer size is proportional to the maximum difference between the number of words produced and the number of words consumed at any point in time. This approach showed significant improvement in power dissipation and silicon area. The buffer size can be further optimized by considering the idle time of buffer. If some buffer is idle at some time instant, it can share the

load of neighbouring input channel and thus increase the utilization of existing resources with small control logic [6].

The author proposed the router architecture with Reliability Aware Virtual Channel (RAVC). In this approach, more memory is allocated to the busy channels and less to the idle channels. This dynamic allocation of storage shows 7.1% and 3.1% latency decrease under uniform and transposes traffic patterns respectively at the expense of complex memory control logic, though this solution is latency efficient but not area and power efficient [7].

III. ROUTING ALGORITHM

Routing methods for network decides the path for data transfer to the destination point. The overview of some methods is provided below.

A. XY Routing Algorithm

Routing algorithm is used to rout the packets from source PE to destination PE. XY routing algorithm is used to rout the packet in proposed router designing. It is a type of kind of distributed deterministic routing algorithms. In 2-D mesh topology NoC, each router can be identified by its coordinate as shown in fig .1. The XY routing algorithm compares the current router address (Cx,Cy) to the destination router address (Dx,Dy) of the packet, stored in the header flit. Flits must be routed to the core port of the router when the (Cx,Cy) address of the current router is equal to the (Dx,Dy) address. If this is not the case, the Dx address is firstly compared to the Cx (horizontal) address. Flits will be routed to the East port when Cx<Dx, to West when Cx>Dx and if Cx=Dx the header flit is already horizontally aligned. If this last condition is true, the Dy (vertical) address is compared to the Cy address. Flits will be routed to South when Cy<Dy, to North when Cy>Dy. If the chosen port is busy, the header flit as well as all subsequent flits of this packet will be blocked. The routing request for this packet will remain active until a connection is established in some future execution of the procedure in this router [8].

B. Surrounding XY Routing

Surrounding XY routing (*S-XY*) has three different routing modes. *N-XY* (*Normal XY*) mode works just like the basic XY routing. It routes packets first along x-axis and then along y-axis. Routing stays on NXY mode as long as network is not blocked and routing does not meet inactive routers [11]. SH-XY (Surround horizontal XY) mode is used when the router's left or right neighbour is deactivated. Correspondly the third mode SV-XY (Surround vertical XY) is used when the upper or lower neighbour of the router is inactive.

The SH-XY mode routes packets to the correct column on the grounds of coordinates of the destination. The algorithm bypasses packets around the inactive routers along the shortest possible path. The situation is a little bit different in the SV-XY mode because the packets are already in the right column. Packets can be routed to left or right. The routers in the SH-XY and SV-XY modes add a small identifier to the packets that tells to other routers that these packets are routed using SH-XY or SV-XY mode [11]. Thus the other routers do not send the packets backwards. Surrounding XY routing is used in a DyNoC. It is a method that supports communication between modules which are dynamically placed on a device.

C. OE Routing Algorithm

OE routing algorithm is a distributed adaptive routing algorithm which is based on odd-even turn model. It has some restrictions, for avoiding and preventing from deadlock appearance [12]. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels.

In a two-dimension mesh with dimensions X*Y each node is identified by its coordinate (x, y). In this model, a column is called even if its x dimension element is even numerical column. Also, a column is called odd if its x dimension element is an odd number. A turn involves a 90-degree change of travelling direction [12]. A turn is a 90-degree turn in the following description. There are eight types of turns, according to the travelling directions of the associated channels. A turn is called an ES turn if it involves a change of direction from East to South. Similarly, we can define the other seven types of turns, namely EN, WS, WN, SE, SW, NE, and NW turns, where E, W, S, and N indicate East, West, South, and North, respectively.

As a whole, there are two conditions [12].

1. No packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column.
2. No packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node which is in an odd column.

IV. SWITCHING METHODES

It is an important method that can determine connections between input port and output port. The crossbar switch is used in most of the router design for providing full connectivity [10]. There are two basic data switching methods.

A. Circuit Switching

In circuit switching routing decision is made when path is set up across the sender and receiver. A dedicated path is established between the sender and receiver which are maintained for the entire duration of transmission [9]. Moreover, links remain occupied even with the absence of data transmission. There is no delay in data flow because of the dedicated path. The major drawback of circuit switching is its limiting scalability.

B. Packet Switching

In packet switching, data is broken up into packets. Individual packets take different routes to reach the destination. Each packet includes a header with source, destination and intermediate node address information. The performance can be increases due segmentation of data.

There are three types of packet switching: warmhole (WH), store and forward (SAF) and virtual cut through (VCT) switching [9].The need to buffer complete packet within a router can make it difficult to construct low area, compact and fast routers. In wormhole switching message packets are also pipelined through the network [10]. A message packet is broken up into flits that the flit is the unit of message flow control. Therefore, input and output buffers at a router are typically large enough to store a few flits.

As we said, in this switching, each packet is divided into equal smaller sections named as flit [1]. Flits are concurrently transferred in the network.

In SAF switching router should have sufficient buffer space to store the entire packet. Router in every hop must wait to receive the entire packet before forwarding header flit to the neighbouring router [9]. So, the buffer size should be large enough to store entire packet which suffers it from larger latency compared with other technique.

V. ROUND ROBIN ARBRITRATION

If multiple packets are arrived at the input channel for same destination then these are scheduled with a round robin arbiter. It will check the priority of the channels decided by arbiter (2). Depending on that channel with first priority will be served first, till other channel will have to wait until it has higher priority. Now the channel served recently will have least priority. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffers.

VI. CONCLUSION

In the current technology enhancement in the utilization of idle resources instead of inserting new ones can make the NoC an ideal solution for current applications.

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